

IN THE CLAIMS:

1. (Currently Amended) A method of manufacturing a semiconductor device, comprising the steps of:
 - forming an island shape semiconductor film over a substrate;
 - forming a first insulating film on the island shape semiconductor film;
 - forming an island shape gate electrode and a capacitor wiring over the island shape semiconductor film with the first insulating film interposed therebetween;
 - forming a second insulating film covering the gate electrode and the capacitor wiring;
 - forming a first contact hole to reach the gate electrode by selectively etching the second insulating film;
 - forming a scanning line to be connected to the gate electrode on the second insulating film;
 - forming a third insulating film on the scanning;
 - forming a second contact hole to reach the semiconductor film by selectively etching the third insulating film;
 - forming a signal line to be electrically connected to the island shape semiconductor film;
 - forming a fourth insulating film over the signal line; and
 - forming a pixel electrode over the ~~pixel electrode~~ fourth insulation film.
2. (Previously presented) The method according to claim 1 wherein said island shape gate electrode and said capacitor wiring comprise a material selected from the group consisting of poly-Si, WSi_x ($x=2.0$ to 2.8), Al, Ta, Cr, Mo.
3. (Previously presented) The method according to claim 1 wherein said second insulating film comprises a material selected from the group consisting of silicon oxide, silicon nitride oxide and silicon nitride.
4. (Previously presented) The method according to claim 1 wherein said scanning line comprises a material selected from the group consisting of W, Cr and Al.

5. (Previously presented) The method according to claim 1 wherein said pixel electrode is transparent.

6. (Currently amended) A method of manufacturing a semiconductor device, comprising the steps of:

- forming a semiconductor film over a substrate;
- forming a first insulating film on the ~~island-shape~~ semiconductor film;
- forming a first conductive film on the first insulating film;
- patterning said first conductive film into an island shape gate electrode and a capacitor wiring over said semiconductor film;
- forming a second insulating film covering the gate electrode and the capacitor wiring;
- forming a first contact hole to reach the gate electrode by selectively etching the second insulating film;
- forming a scanning line to be connected to the gate electrode on the second insulating film;
- forming a third insulating film on the scanning;
- forming a signal line to be electrically connected to the semiconductor film;
- forming a fourth insulating film over the signal line; and
- forming a pixel electrode over the ~~pixel electrode~~ fourth insulation film.

7. (Previously presented) The method according to claim 6 wherein said first conductive film comprises a material selected from the group consisting of poly-Si, WSi_x ($x=2.0$ to 2.8), Al, Ta, Cr, Mo.

8. (Previously presented) The method according to claim 6 wherein said second insulating film comprises a material selected from the group consisting of silicon oxide, silicon nitride oxide and silicon nitride.

9. (Previously presented) The method according to claim 6 wherein said scanning line comprises a material selected from the group consisting of W, Cr and Al.

10. (Previously presented) The method according to claim 6 wherein said pixel electrode is transparent.

11. (Currently amended) A method of manufacturing a semiconductor device, comprising the steps of:

forming a first insulating film on a first semiconductor region to become a channel region of a thin film transistor and a second semiconductor region to become a capacitor electrode;

forming a first conductive film on the first insulating film;

patterning said first conductive film into an island shape gate electrode over the first semiconductor region and a capacitor wiring over the second semiconductor region;

forming a second insulating film covering the gate electrode and the capacitor wiring;

forming a first contact hole to reach the gate electrode by selectively etching the second insulating film;

forming a scanning line to be connected to the gate electrode on the second insulating film through said first contact hole;

forming a third insulating film on the scanning;

forming a signal line to be electrically connected to the semiconductor film;

forming a fourth insulating film over the signal line; and

forming a pixel electrode over the ~~pixel-electrode~~ fourth insulation film.

12. (Previously presented) The method according to claim 11 wherein said first semiconductor region and said second semiconductor region are contiguous to each other.

13. (Previously presented) The method according to claim 11 further comprising adding an impurity to said second semiconductor region for giving one of N-type or P-type conductivity thereto.

14. (Previously presented) The method according to claim 11 wherein said first conductive film comprises a material selected from the group consisting of poly-Si, WSi_x ($x=2.0$ to 2.8), Al, Ta, Cr, Mo.

15. (Previously presented) The method according to claim 11 wherein said second insulating film comprises a material selected from the group consisting of silicon oxide, silicon nitride oxide and silicon nitride.

16. (Previously presented) The method according to claim 11 wherein said scanning line comprises a material selected from the group consisting of W, Cr and Al.

17. (Previously presented) The method according to claim 11 wherein said pixel electrode is transparent.

18. (Previously presented) A method of manufacturing a semiconductor device, comprising the steps of:

forming a first insulating film on a first semiconductor region to become a channel region of a thin film transistor and a second semiconductor region to become a capacitor electrode;

forming a first conductive film on the first insulating film;

patterning said first conductive film into an island shape gate electrode over the first semiconductor region and a capacitor wiring over the second semiconductor region;

forming a second insulating film covering the gate electrode and the capacitor wiring;

forming a first contact hole to reach the gate electrode by selectively etching the second insulating film;

forming a scanning line to be connected to the gate electrode on the second insulating film;

forming a third insulating film on the scanning line;

forming a signal line to be electrically connected to the semiconductor film, wherein said signal line extends in parallel with said capacitor wiring.

19. (Currently amended) The method according to claim 18 further comprising steps of:

forming a fourth insulating film over the signal line; and

forming a pixel electrode over the ~~pixel electrode~~ fourth insulation film.

20. (Previously presented) The method according to claim 18 wherein said first semiconductor region and said second semiconductor region are contiguous to each other.

21. (Previously presented) The method according to claim 18 further comprising adding an impurity to said second semiconductor region for giving one of N-type or P-type conductivity thereto.

22. (Previously presented) The method according to claim 18 wherein said first conductive film comprises a material selected from the group consisting of poly-Si, WSi_x ($x=2.0$ to 2.8), Al, Ta, Cr, Mo.

23. (Previously presented) The method according to claim 18 wherein said second insulating film comprises a material selected from the group consisting of silicon oxide, silicon nitride oxide and silicon nitride.

24. (Previously presented) The method according to claim 18 wherein said scanning line comprises a material selected from the group consisting of W, Cr and Al.